

Talha Ahmed

Last updated in Aug 2026

Software Engineer — Hardware Security

📍 Karachi, Pakistan ✉ tahmed@uitu.edu.pk ☎ +92-302-2601500 in talha-a-316a68113 🌐 talha-ahmed-1

Education

Sungkyunkwan University

MS in Electrical and Computer Engineering

Aug 2023 – Aug 2025

- GPA: 3.67/4.5
- **Coursework:** Advanced Algorithms, ML Security and Robustness, OS Design
- **Research Area:** Sparse Matrix Multiplication Algorithms, Secure Computer Architecture

UIT University

BS in Software Engineering

Aug 2018 – Aug 2022

- GPA: 3.1/4.0
- **Coursework:** OOP, Data Structures and Algorithms, Software QA, Artificial Intelligence
- **Research Area:** Computer Architecture, Digital Logic Design

Technologies

Languages: C, Python, CUDA, Scala, CHISEL, Verilog, Assembly

Technologies: Git, Linux, RISC-V ISA, Chipyard, Vivado

Experience

Software Team Lead

Sept 2025 – Present

Research Fellow

Sept 2019 – Aug 2023

Micro Electronics Research Lab - MERL

Karachi, Pakistan

- Designed a Web-based System on Chip (SoC) Generator in Django.
- Designed RV-C extension Compressed Assembler in Python.
- Automate SoC generation and verification flow in Scala and Python.
- Involved in reverse engineering of Rocket Chip.

Lecturer

Sept 2025 – Present

UIT University

Karachi, Pakistan

Taught the following courses:

- Data Structures and Algorithms (Theory + Practical).
- Computer Organization and Assembly Language (Theory + Practical).
- Software Requirements Engineering (Theory).
- Software Construction Development (Theory + Practical).
- Software Quality Engineering (Theory).

Research Fellow

Sept 2023 – Aug 2025

Computer Architecture and Systems Lab - COMPASS LAB SKKU

Suwon, South Korea

- Server setup for Firesim with Alveo-U280 FPGA for cloud-based FPGA acceleration.
- Evaluate and optimize multiple sparse **Matrix** multiplication algorithms on GPU using CUDA.
- Improving the security and performance by minimizing the overhead for NVMe based storage.

RISC-V CPU Designer

Oct 2022 – Sept 2023

Internee

July 2022 – Sept 2022

Intensivate

Berkeley, California (Remote)

- Integrate memory system IP with the Rocket Chip based server class CPU in CHISEL.
- Design and integrate GPIO in SoC with appropriate cells.
- Verify the integration of SRAM based memory IPs in RTL.
- Added new MMIO modules to Rocket Chip for better understanding the RTL generation flow.

Google Summer of Code 2022

June 2022 – Sept 2022

Center for Research in Open Source Software - CROSS

Santa Cruz, California (Remote)

- Implement the digital design of the latch-based register file.
- Extend OpenRAM memory compiler for register file generation.

- Use open source Skywater PDKs for compilation and fix DRC and LVS issues.

Publications

An Experimental Study of Merkle Tree-Based Security Mechanism for Secure SSD Storages

Osaka, Japan

Talha Ahmed and Seokin Hong

2025 International Conference on Electronics, Information, and Communication (ICEIC)

[10.1109/ICEIC64972.2025.10879627](https://doi.org/10.1109/ICEIC64972.2025.10879627) [🔗](#)

Achievement

Tape-out: Multi Project Wafer 6

Github: [soc-now-mpw6](#) [🔗](#)

SoCNow generated SoC is taped out in Google sponsored MPW-6.

STEM Scholarship

Fully funded Master's scholarship in Sungkyunkwan University, South Korea

Mentorship

Linux Foundation Mentorship Program 2022 & 2026 (RISC-V Sponsored) - Mentor

Project [1](#) [🔗](#) & [2](#) [🔗](#)

Project 1 "Open-source RISC-V Vector accelerated sparse linear algebra library."

Project 2 "Addition of Single Precision Floating Point (F) extension in NucleusRV"

Google Summer of Code 2025 - Mentor

Project [1](#) [🔗](#) & [2](#) [🔗](#)

Project 1 "Running Secure and Vectorized Applications on SoC-Now"

Project 2 "AEGIS - AI-Enhanced Generation of Intelligent Scenarios"

Google Summer of Code 2022 - Mentee

[Blog](#) [🔗](#)

Project "Register File Generator" under supervision of CROSS - UC Santa Cruz.

Projects

SafeSSD: Treeless SSD Protection by Leveraging Physical Address as Version Number

Postgrad. Thesis

- Experimentally analyze metadata overhead associated with tree-based SSD security.
- Proposed a security method eliminating the need for Merkle trees, a common source of overhead in SSD security.
- Introduce on-drive integrity check, improves flash cell endurance along with performance.
- Tools Used: C++, Python, MQSim

SoC-Now: Open Source Web based RISC-V SoC Generator.

Github: [SoC-Now](#) [🔗](#)

Undergrad. Thesis

- Developed a web app in Django for automated SoC generation and emulation.
- Design plug-and-play SoC components, made configurations parametrized with Scala, and integrated verification flow.
- Integrated FPGA automation interface in web app.
- Tools Used: Python, Django, Scala, CHISEL

OpenRegFile: Open Source Register File Generator

[GSoC'22](#) [🔗](#)

- Extended the OpenRAM memory compiler to automate latch-based register file generation using Skywater 130nm standard cells.
- OpenRegFile produces spice netlists, layouts, and Verilog models, utilizing hierarchical decoders and muxes from SRAM designs.
- Tools Used: Python, OpenRAM, Magic, Netgen

Workshop and Presentation

Pakistan Semiconductor Summit 2026

Technical Session [🔗](#)

SoC-Now: An Open-Source RISC-V SoC Generation Framework from RTL to Silicon

Design Automation Conference DAC'25

WiP Poster [🔗](#)

SafeSSD: Treeless SSD Protection by Leveraging Physical Address as Version Number

RISC-V Summit Europe 2023

Extended Abstract [🔗](#)

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

First Firesim and Chipyard User and Developer Workshop at ASPLOS'23

[Workshop](#) 

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

Workshop on Open Source EDA Technology - WOSET'22

[Workshop](#) 

- SoC-Now: An Open-Source Web based RISC-V SoC Generator
- Bitstream Chef
- OpenRegFile: Open-Source Register File Generation

RISC-V International Summit 2020

[Presentation](#) 

Reverse Engineering of Rocket Chip

Extras

Technical Report Writing for Engineers: *Future Learn, University of Sheffield.*

[Certificate](#) 

XOR Linked List Data Structure:

[Article](#) 